memory elements arranged in the array, the non-volatile semiconductor memory elements arranged in the first direction, each of widths of the formed second semiconductor or insulator layer and the formed second upper electrode being greater than a width of the second shared electrode, and each of the second semiconductor or insulator layer and the second upper electrode being plurally formed in parallel corresponding to the non-volatile semiconductor memory elements arranged in the first direction,

wherein, in each of the forming of the plurality of first shared electrodes by nitriding the front surfaces of the plurality of first variable resistance layers and the forming of the plurality of second shared electrodes by nitriding the front surfaces of the second variable resistance layers, the front surfaces of the second variable resistance layers are nitrided to replace oxygen atoms in front surface parts of the first and second variable resistance layers with nitrogen atoms so that the front surfaces of the first and second variable resistance layers form the shared electrodes comprising the nitride of the transition metal,

the front surface of the shared electrode comprises the nitride of the transition metal including the transition metal and nitrogen, so that a Schottky barrier is formed in an interfacial surface between the shared electrode and the semiconductor or insulator layer, and

processes (a) to (l) correspond to a basic unit of processing, and a plurality of stacked structures are formed by repeating (b) to (l) after performing (l), each of the stacked structures including the variable resistance element and the non-ohmic element stacked on the variable resistance element.

17. The method of manufacturing the non-volatile semiconductor memory device according to claim **16**,

wherein the oxide of the transition metal is one of a tantalum oxide and a hafnium oxide, and

a front surface of the one of the tantalum oxide and the hafnium oxide is nitrided so as to form the shared electrode having a front surface comprising a corresponding one of a tantalum nitride and a hafnium nitride.

18. The method of manufacturing the non-volatile semiconductor memory device according to claim **16**,

wherein the variable resistance layer includes:

a first transition metal oxide layer formed on the first electrode; and

a second transition metal oxide layer that is formed on the first transition metal oxide layer and has a lower oxygen content atomic percentage than the first transition metal oxide layer.

19. The method of manufacturing the non-volatile semiconductor memory element according to claim **10**,

wherein, in the forming of the shared electrode, the front surface of the oxide of the transition metal is nitrided according to the plasma nitriding process so as to form the shared electrode comprising the nitride of the transition metal.

20. The method of manufacturing the non-volatile semiconductor memory element according to claim **10**,

wherein the plasma nitriding process for forming the shared electrode is performed under an application of heat of 400 degrees centigrade or higher.

21. The method of manufacturing the non-volatile semiconductor memory element according to claim **10**,

wherein the plasma nitriding process for forming the shared electrode is performed for 180 seconds or longer.

22. The method of manufacturing the non-volatile semiconductor memory device according to claim **13**,

wherein, in the forming of the shared electrode, the front surface of the oxide of the transition metal is nitrided according to the plasma nitriding process so as to form the shared electrode comprising the nitride of the transition metal.

23. The method of manufacturing the non-volatile semiconductor memory device according to claim **13**,

wherein the plasma nitriding process for forming the shared electrode is performed under an application of heat of 400 degrees centigrade or higher.

24. The method of manufacturing the non-volatile semiconductor memory device according to claim **13**,

wherein the plasma nitriding process for forming the shared electrode is performed for 180 seconds or longer.

25. The method of manufacturing the non-volatile semiconductor memory device according to claim **16**,

wherein, in the forming of the shared electrode, the front surface of the oxide of the transition metal is nitrided according to the plasma nitriding process so as to form the shared electrode comprising the nitride of the transition metal.

26. The method of manufacturing the non-volatile semiconductor memory device according to claim **16**,

wherein the plasma nitriding process for forming the shared electrode is performed under an application of heat of 400 degrees centigrade or higher.

27. The method of manufacturing the non-volatile semiconductor memory device according to claim **16**,

wherein the plasma nitriding process for forming the shared electrode is performed for 180 seconds or longer.

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